Amendments t the Claims: This listing of claims will replace all prior versions, and listings, of claims in the application

Listing of Claims:

1. (Currently Amended) A semiconductor differential circuit comprising:

a semiconductor substrate,

a first semiconductor device formed on said semiconductor substrate, having a first gate electrode for having one of differential signals conveyed thereto and a first drain electrode for outputting one of the differential signals controlled by said first gate electrode;

a second semiconductor device formed on said semiconductor substrate, having a second gate electrode for having the other of said differential signals conveyed thereto and a second drain electrode for outputting the other of the differential signals controlled by said second gate electrode, and wherein:

said first drain electrode and said second drain electrode are placed in ~~the~~ proximity so that, at a predetermined frequency, it is equivalent to the one in which said first drain electrode is grounded via a first predetermined resistance, and said second drain electrode is grounded via a resistance of the same resistance value as said first predetermined resistance.

2. (Original) The semiconductor differential circuit according to claim 1, wherein the resistance value of said first predetermined resistance is half the resistance value formed between said first drain electrode and said second drain electrode via said semiconductor substrate, which is determined by space between said first drain electrode and said second drain electrode at said predetermined frequency.

3. (Original) The semiconductor differential circuit according to claim 1, wherein said first semiconductor device and said second semiconductor device are multi-finger type FETs respectively, and are placed so that a longitudinal direction of said second drain electrode is along and in the proximity of the longitudinal direction of said first drain electrode.

4. (Original) The semiconductor differential circuit according to claim 3, wherein:

as to said first semiconductor device:

said first gate electrode is placed to be adjacent to said first drain electrode along the longitudinal direction of said first drain electrode; and

it has a first source electrode placed to be adjacent to said first gate electrode along the longitudinal direction of said first gate electrode, and

as to said second semiconductor device:

said second gate electrode is placed to be adjacent to said second drain electrode along the longitudinal direction of said second drain electrode; and

it has a second source electrode placed to be adjacent to said second gate electrode along the longitudinal direction of said second gate electrode, and

a circuit comprising said first semiconductor device and said second semiconductor device is provided as a first unit circuit;

n pieces of said first unit circuit are placed to be mutually adjacent;

an i + 1-th first unit circuit is placed to be adjacent to an i-th (i is between 1 and n - 1) first unit circuit; and

said n pieces of first drain electrode are mutually connected, said n pieces of second drain electrode are mutually connected, said n pieces of first gate electrode are mutually connected, said n pieces of second gate electrode are mutually connected, and said n pieces of first source electrode and said n pieces of second source electrode are mutually connected.

5. (Original) The semiconductor differential circuit according to claim 3, wherein:

a third source electrode is formed on said semiconductor substrate;

said first gate electrode is placed to be adjacent to said third source electrode along the longitudinal direction of said third source electrode;

said first drain electrode is placed in the proximity of said first gate electrode on the opposite side to said third source electrode along the longitudinal direction of said first gate electrode;

said second drain electrode is placed to be adjacent to said first drain electrode on the opposite side to said first gate electrode along the longitudinal direction of said first drain electrode;

said second gate electrode is placed to be adjacent to said second drain electrode on the opposite side to said first drain electrode along the longitudinal direction of said second drain electrode, and

a circuit comprising said third source electrode, said first gate electrode, said first drain electrode, said second drain electrode and said second gate electrode is provided as a second unit circuit;

n pieces of said second unit circuit are placed to be mutually adjacent;

said second gate electrode of the i-th (i is between 1 and n - 1) second unit circuit is placed to be adjacent to said third source electrode of the i + 1-th second unit circuit; and

said n pieces of first drain electrode are mutually connected, said n pieces of second drain electrode are mutually connected, said n pieces of first gate electrode are mutually connected, said n pieces of second gate electrode are mutually connected, and said n pieces of third source electrode are mutually connected.

6. (Original) The semiconductor differential circuit according to claim 1, wherein:

said first gate electrode is placed to surround said first drain electrode;

said second gate electrode is placed to surround said second drain electrode; and

a source electrode is placed between said first gate electrode and said second gate electrode.

7. (Original) The semiconductor differential circuit according to claim 6, wherein:

there are two pieces each of said first drain electrode and said second drain electrode;

a source electrode is placed between one first drain electrode and one second drain electrode;

an electrode connected to said source electrode is placed between the other first drain electrode and the other second drain electrode;

an electrode connected to said source electrode is placed between one first drain electrode and the other second drain electrode; and

an electrode connected to said source electrode is placed between the other first drain electrode and said one second drain electrode.

8. (Original) The semiconductor differential circuit according to claim 1 or 2, wherein:

said first gate electrode is placed to be adjacent to said first drain electrode;

said second gate electrode is placed to be adjacent to said second drain electrode; and

a source electrode is placed to surround said first drain electrode, said second drain electrode, said first gate electrode and said second gate electrode and to be adjacent to said first gate electrode and said second gate electrode.

9. (Original) The semiconductor differential circuit according to claim 8, wherein there are two pieces each of said first drain electrode and said second drain electrode, and one first drain electrode and one second drain electrode are placed to be in proximity, the other first drain electrode and the other second drain electrode are placed to be in proximity, said one first drain electrode and said other second drain electrode are placed to be in proximity, and said other first drain electrode and said one second drain electrode are placed to be in proximity.

10. (Original) A semiconductor differential circuit comprising:

a semiconductor substrate,

a first semiconductor device, formed on said semiconductor substrate, having a first collector or base for having one of differential signals conveyed thereto; and

a second semiconductor device, formed on said semiconductor substrate, having a second collector or base for having the other of said differential signals conveyed thereto, and wherein:

said first collector or base and said second collector or base are placed in the proximity so that, at a predetermined frequency, it is equivalent to the one in which said first collector or base is grounded via a second predetermined resistance, and said second collector or base is

grounded via a resistance of the same resistance value as said second predetermined resistance.

11. (Original) An oscillation apparatus using the semiconductor differential circuit according to claim 1 or 10.

12. (Original) A switching apparatus using the semiconductor differential circuit according to claim 1 or 10.

13. (Original) An amplifying apparatus using the semiconductor differential circuit according to claim 1 or 10.

14. (Original) A semiconductor differential circuit placement method comprising the steps of:

forming on a semiconductor substrate a first semiconductor device having a first drain electrode for having one of differential signals conveyed thereto and a first gate electrode for controlling said one of the signals;

forming on said semiconductor substrate a second semiconductor device having a second drain electrode for having the other of said differential signals conveyed thereto and a second gate electrode for having said other signal conveyed thereto formed, and wherein:

said first drain electrode and said second drain electrode are placed in the proximity so that, at a predetermined frequency, it is equivalent to the one in which said first drain electrode is grounded via a first predetermined resistance, and said second drain electrode is grounded via a resistance of the same resistance value as said first predetermined resistance.

15. (Currently Amended) The semiconductor differential circuit according to claim 1, wherein:

it further comprises:

a third semiconductor device, formed on said semiconductor substrate, having a second gate electrode for having the other of said differential signals conveyed thereto, and a first drain electrode for outputting one of the differential signals controlled by said second gate electrode; and

a fourth semiconductor device, formed on said semiconductor substrate, having a first gate electrode for having one of said differential signals conveyed thereto, and a second drain electrode for outputting the other of the differential signals controlled by said first gate electrode, and

the differential signals conveyed to said first gate electrode and said second gate electrode are differential local oscillation signals;

said first semiconductor device has a first source electrode for having one of the differential signals to be mixed with said differential local oscillation signals conveyed thereto;

said second semiconductor device shares said first source electrode with said first semiconductor device;

said third semiconductor device shares said first drain electrode with said first semiconductor device, and has a second source electrode for having the other of the differential signals to be mixed with said differential local oscillation signals conveyed thereto;

said fourth semiconductor device shares said second source electrode with said third semiconductor device, and shares said second drain electrode with said second semiconductor device;

said differential signals controlled by said second gate electrode are the differential signals having said differential local oscillation signals and said differential signals to be mixed ~~mixed~~ therein; and

said first drain electrode and said second drain electrode are placed in the proximity so that, at a frequency of said mixed differential signals, it is equivalent to the one in which said first drain electrode is grounded via a first predetermined resistance, and said second drain electrode is grounded via a resistance of the same resistance value as said first predetermined resistance.

16. (Original) The semiconductor differential circuit according to claim 15, wherein:

said first gate electrode and said second gate electrode are placed in the proximity so that, at a frequency of said differential local oscillation signals, it is equivalent to the one in which said first gate electrode is grounded via a third predetermined resistance, and said second gate electrode is grounded via a resistance of the same resistance value as said third predetermined resistance; and

said first source electrode and said second source electrode are placed in the proximity so that, at a frequency of the differential signals to be mixed with said differential local oscillation signals, it is equivalent to the one in which said first source electrode is grounded via a fourth predetermined resistance, and said second source electrode is grounded via a resistance of the same resistance value as said fourth predetermined resistance.

17. (Original) The semiconductor differential circuit according to claim 15, wherein the resistance value of said first predetermined resistance is half the resistance value formed between said first drain electrode and said second drain electrode via said semiconductor substrate, which is determined by space between said first drain electrode and said second drain electrode at the frequency of said mixed differential signals.

18. (Original) The semiconductor differential circuit according to claim 16, wherein the resistance value of said third predetermined resistance is half the resistance value formed between said first gate electrode and said second gate electrode via said semiconductor substrate, which is determined by space between said first gate electrode and said second gate electrode at the frequency of said differential local oscillation signals.

19. (Original) The semiconductor differential circuit according to claim 16, wherein the resistance value of said fourth predetermined resistance is half the resistance value formed between said first source electrode and said second source electrode via said semiconductor substrate, which is determined by space between said first source electrode and said second source electrode at the frequency of the differential signals to be mixed.

20. (Original) The semiconductor differential circuit according to claim 15, wherein said first semiconductor device, said second semiconductor device, said third semiconductor device and said fourth semiconductor device are multi-finger type FETs respectively, and are placed so that a longitudinal direction of said second drain electrode is along and in the proximity of the longitudinal direction of said first drain electrode.

21. (Original) The semiconductor differential circuit according to claim 16, wherein said first semiconductor device, said second semiconductor device, said third semiconductor device and said fourth semiconductor device are multi-finger type FETs respectively, and are placed so that a longitudinal direction of said second gate electrode is along and in the proximity of the longitudinal direction of said first gate electrode.

22. (Original) The semiconductor differential circuit according to claim 16, wherein said first semiconductor device, said second semiconductor device, said third semiconductor device and said fourth semiconductor device are multi-finger type FETs respectively, and are placed so that a longitudinal direction of said second source electrode is along and in the proximity of the longitudinal direction of said first source electrode.

23. (Original) The semiconductor differential circuit according to any one of claim 20 to 22, wherein:

the first source electrode is formed on said semiconductor substrate;

said first gate electrode is placed to be adjacent to said first source electrode along the longitudinal direction of said first source electrode; and

said first drain electrode is placed to be adjacent to said first gate electrode on the opposite side to said first source electrode along the longitudinal direction of said first gate electrode;

said second gate electrode is placed to be adjacent to said first drain electrode on the opposite side to said first gate electrode along the longitudinal direction of said first drain electrode;

said second source electrode is placed to be adjacent to said second gate electrode on the opposite side to said first drain electrode along the longitudinal direction of said second gate electrode;

said first gate electrode is placed to be adjacent to said second source electrode on the opposite side to said second gate electrode along the longitudinal direction of said second source electrode;

said second drain electrode is placed to be adjacent to said first gate electrode on the opposite side to said second source electrode along the longitudinal direction of said first gate electrode;

said second gate electrode is placed to be adjacent to said second drain electrode on the opposite side to said first gate electrode along the longitudinal direction of said second drain electrode, and

a circuit having said first source electrode, said second source electrode, said first gate electrode, said second gate electrode, said first drain electrode and said second drain electrode is provided as a third unit circuit;

n pieces of said third unit circuit are placed to be mutually adjacent;

said second gate electrode of an i-th (i is between 1 and n - 1) third unit circuit is placed to be adjacent to said first source electrode of an i + 1-th third unit circuit; and

said n pieces of first drain electrode are mutually connected, said n pieces of second drain electrode are mutually connected, said n pieces of first gate electrode are mutually connected, said n pieces of second gate electrode are mutually connected, said n pieces of first source electrode are mutually connected, and said n pieces of second source electrode are mutually connected.

24. (Original) A mixer apparatus using the semiconductor differential circuit according to any one of claim 1, 10 and 15.

25. (Original) A circuit apparatus sharing an FET source, using the semiconductor differential circuit according to claim 1.

Respectfully submitted,

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